Please add the following:

126. The capacitor of claim 1, wherein the dielectric layer directly adjoins the first electrode, and the metal oxide buffer layer directly adjoins the dielectric layer and the second electrode.

127. The capacitor of claim 1, wherein the dielectric layer comprises a single layer.

REMARKS

Claims 1, 9, 12, 16, 20, 23, 25, 26, 28, 30, 73-77, 79-81, 83-88, 90-94, 96-100, 102-106, 110, 113, 116, 118, and 124 are amended, no claims are canceled, and claims 126-127 are added; as a result, claims 1-232, 73-106, and 110-127 are now pending in this application.

§102 Rejection of the Claims

Claims 1-32 and 106 were rejected under 35 USC § 102(b) as being anticipated by Horiike et al. (U.S. Patent No. 5,290,609). Applicant respectfully traverses.

With respect to claim 1, it recites, in part, a single compound dielectric layer and a buffer layer intermediate the dielectric layer and one of the first and second electrodes. In contrast to claim 1, Horiike describes a multilayer, multi-compound dielectric layer, which is needed to prevent leakage through the dielectric layer. As Horiike does not teach all of the features of claim 1, applicant requests that the anticipation rejection be withdrawn. Moreover, dependent claims 2-4 are believed to be allowable at least because they depend from claim 1.

Further, applicant traverses the rejection of claim 4, under § 102(b) based on Horiike and Oshida. The office action states that claim 4 is anticipated by Horiike disclosing the buffer may be formed from titanium oxide, which is understood in the art to be able to be formed with an orthorhombic crystal structure, for example as recited in Oshida. First, applicant traverses the multiple reference §102 rejection as the office action admits that Horiike does not disclose all of the features of claim 4. Moreover, applicant further traverse the assertion that Oshida is "in the art." Oshida is directed to a titanium material medical implant. The present invention is directed to an integrated circuit structure. Obviously, these are not the same art. Still further, applicant

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respectfully traverses this assertion as a form of official notice and requests a reference to support the assertion or withdrawal of the assertion according to MPEP 2144.03.

With respect to claim 5, applicant respectfully traverses. Claim 5 includes the buffer layer being tungsten trioxide. Applicant can not find where Horiike discloses tungsten trioxide. The office action points to col. 7, line 12 as a teaching of tungsten oxide. However, this passage does not teach tungsten *trioxide*. As Horiike does not teach all of the features of claim 5, applicant requests that the rejection under §102 be withdrawn.

Moreover, claims 6-8 are believed to be allowable at least because they depend from claim 5.

Claims 9-32 and 106 are believed to be allowable over Horiike for substantially similar reasons as stated above with regard to claim 1.

§103 Rejection of the Claims

Claims 73-80 were rejected under 35 USC § 103(a) as being unpatentable over Ino (U.S. Patent No. 4,899,203) in view of Horiike et al. Applicant traverses. The Office Action admits that Ino does not disclose the capacitor as recited in the claim. The Office relies on Horiike for a teaching of a capacitor. However, claims 73-80 are believed distinguished over Horiike for substantially similar reasons as stated above. As Ino and Horiike, either alone or in combination, doe not teach all of the elements as recited in the claims, applicant requests that the rejection be withdrawn.

Claims 81-87 and 110-117 were rejected under 35 USC § 103(a) as being unpatentable over Yoneda (U.S. Patent No. 5,177,574) in view of Horiike et al. The Office Action admits that Yoneda does not disclose the capacitor as recited in the claim. The Office relies on Horiike for a teaching of a capacitor. However, claims 81-87 and 110-117 are believed distinguished over Horiike for substantially similar reasons as stated above. As Yoneda and Horiike, either alone or in combination, doe not teach all of the elements as recited in the claims, applicant requests that the rejection be withdrawn.

Claims 88-93 were rejected under 35 USC § 103(a) as being unpatentable over Chu et al. (U.S. Patent No. 5,856,937) in view of Horiike et al. The Office Action admits that Chu does not

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disclose the capacitor as recited in the claim. The Office relies on Horiike for a teaching of a capacitor. However, claims 88-93 are believed distinguished over Horiike for substantially similar reasons as stated above. As Chu and Horiike, either alone or in combination, doe not teach all of the elements as recited in the claims, applicant requests that the rejection be withdrawn.

Claims 94-105 and 118-125 were rejected under 35 USC § 103(a) as being unpatentable over Le et al. (U.S. Patent No. 5,867,444) in view of Horiike et al. The Office Action admits that Le does not disclose the capacitor as recited in the claim. The Office relies on Horiike for a teaching of a capacitor. However, claims 88-93 are believed distinguished over Horiike for substantially similar reasons as stated above. As Le and Horiike, either alone or in combination, doe not teach all of the elements as recited in the claims, applicant requests that the rejection be withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SAM YANG

By their Representatives,

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Date 30 Dec 2002 By

Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 30th day of December, 2002.

Name Amy Moriarty

Signature

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Docket No. 303.714US1
WD # 465620

Micron Ref. No. 00-0385

Clean Version of Pending Claims

LOW LEAKAGE MIM CAPACITOR
Applicant: Sam Yang
Serial No.: 09/745,114

Claims 1-32, 73-106, and 110-127, as of December 30, 2002 (Date of Response to First Office Action filed).

1. (Amended) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes.

2. The capacitor according to claim 1, wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

3. The capacitor according to claim 2, wherein the dielectric layer is a tantalum oxide.

4. The capacitor according to claim 1, wherein the buffer layer has a orthorhomic crystalline structure.

7. ~~5.~~ A capacitor, comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a tungsten trioxide buffer layer interposed between the dielectric layer and one of the first and second electrodes.

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8. ~~6.~~ The capacitor according to claim ~~5~~ 7, wherein the buffer layer has a orthorhomic crystalline structure.

9. ~~7.~~ The capacitor according to claim ~~5~~ 7, wherein the one electrode includes tungsten.

10. ~~8.~~ The capacitor according to claim ~~7~~ 9, wherein the buffer layer is grown by oxidizing the one electrode.

11. ~~9.~~ (Amended) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer interposed between the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

B1 cont.

12. ~~10.~~ The capacitor according to claim ~~9~~ 11, wherein the buffer layer is of the formula MO_x, and M is a metal component from a group consisting of tungsten, tantalum, zirconium, and hafnium.

13. ~~11.~~ The capacitor according to claim ~~9~~ 11, wherein the buffer layer has a orthorhomic crystalline structure.

14. ~~12.~~ (Amended) A vertical capacitor, comprising:

a bottom electrode;

a top electrode positioned above the bottom electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom

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electrode; and

a metal oxide buffer layer intermediate the dielectric layer and the bottom electrode.

15. ~~13.~~ The capacitor according to claim 14 ~~12~~, wherein the bottom electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

16. ~~14.~~ The capacitor according to claim 15 ~~13~~, wherein the dielectric layer is a tantalum oxide.

17. ~~15.~~ The capacitor according to claim 14 ~~12~~, wherein the buffer layer has a orthorhomic crystalline structure.

B1 cont.

18. ~~16.~~ (Amended) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate the dielectric layer and the bottom electrode, wherein the metal in the buffer layer is a refractory metal.

19. ~~17.~~ The capacitor according to claim 18 ~~16~~, wherein the metal in the buffer layer is tungsten.

20. ~~18.~~ The capacitor according to claim 19 ~~17~~, wherein the bottom electrode comprises a metal nitride, and the metal in the bottom electrode is a refractory metal.

21. ~~19.~~ The capacitor according to claim 20 ~~18~~, wherein the bottom electrode comprises tungsten nitride.

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22. ~~20.~~ (Amended) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

a metal oxide buffer layer intermediate the dielectric layer and the bottom electrode, wherein the bottom electrode comprises a metal nitride having a metal component which is the same as the metal component of the metal oxide buffer layer.

B' cont. 23. ~~21.~~ The capacitor according to claim 22 ~~20~~, wherein the dielectric layer comprises tantalum oxide.

24. ~~22.~~ The capacitor according to claim 23 ~~21~~, wherein the metal component of the bottom electrode and the buffer layer includes tungsten.

25. ~~23.~~ (Amended) A capacitor, comprising:

a bottom electrode;

a top electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

wherein at least one electrode selected from the group consisting of the bottom electrode and the top electrode comprises tungsten nitride.

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26. ~~24.~~ The capacitor according to claim 25 ~~23~~, wherein the dielectric layer is a metal oxide of a different type than the buffer layer.

27. ~~25.~~(Amended) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, tantalum oxide dielectric layer interposed between the bottom electrode and the top electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

B' cont.

wherein at least one electrode is selected from the group consisting of the bottom electrode and the top electrode includes tungsten nitride.

28. ~~26.~~(Amended) A capacitor, comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer has an orthorhomic crystal structure.

29. ~~27.~~ The capacitor according to claim 28 ~~26~~, wherein the metal in the buffer layer is tungsten.

30. ~~28.~~ (Amended) A capacitor, comprising:

a bottom electrode;

a top electrode;

B

a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

an annealed metal oxide buffer layer intermediate the dielectric layer and the bottom electrode.

31. ~~29.~~ The capacitor according to claim 30 ~~28~~, wherein the bottom electrode comprises a metal nitride and has a metal component which is the same as the metal component of the metal oxide buffer layer.

32. ~~30.~~ (Amended) A capacitor, comprising:

B1 cont.

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes;

wherein the buffer layer has a dielectric constant greater than the dielectric layer.

33. ~~31.~~ The capacitor according to claim 32 ~~30~~, wherein the one of the first and second electrodes has a metal component which is the same as the metal component of the buffer layer.

34. ~~32.~~ The capacitor according to claim 32 ~~30~~, wherein the buffer layer has an orthorhomic crystalline structure.

35. ~~33.~~ (Amended) A semiconductor die, comprising:

B2

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices

B

comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

36. ~~74.~~ (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

B2 CONT.

37. ~~75.~~ (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

B3

a second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein at least one electrode selected from the group consisting of the first electrode and the second electrode comprises tungsten nitride.

B2 Cont. 38. ~~76.~~ (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a tungsten nitride second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

a tungsten oxide buffer layer is interposed between the dielectric layer and the second electrode.

39. ~~77.~~ (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

B3

a tungsten nitride second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

a high temperature annealed, tungsten oxide buffer layer is interposed between the dielectric layer and the second electrode.

40. ~~78.~~ The semiconductor die according to claim 39 ~~77~~, wherein the high temperature annealed buffer layer is annealed at least 700 degrees Celsius and has an orthorhomic crystal structure.

41. ~~79.~~ (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer is interposed between the dielectric layer and the second electrode,

wherein the buffer layer has an orthorhomic crystal lattice structure.

42. ~~80.~~ (Amended) A semiconductor die, comprising:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

B cont.

B

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer is interposed between the dielectric layer and the second electrode,

wherein the buffer layer has a dielectric constant greater than the dielectric layer.

43. ~~81.~~ (Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

42 cont.

44. ~~82.~~ The memory device according to claim 43 ~~81~~, wherein the electrode selected from the group consisting of the first electrode and the second electrode has a metal component that is the same as the metal component of the buffer layer.

45. ~~83.~~ (Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

B

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

B2 cont.

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

46.
~~84.~~ (Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, wherein at least one electrode selected from the group consisting of the bottom electrode of the capacitor and the top electrode of the capacitor comprises tungsten nitride;

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a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

47.
~~85.~~(Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhomic crystalline structure;

A2 Cont

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

48.
~~86.~~ (Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer interposed between the dielectric layer

B

and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

49.
~~87.~~ (Amended) A memory device, comprising:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

B2 cont.

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one, high temperature annealed, metal oxide buffer layer interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

50.
~~88.~~ (Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality

B

of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

B2 cont.

51. ~~89.~~ The module according to claim ~~88~~ 50, wherein the electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer.

52. ~~90.~~ (Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

B3

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the bottom electrode and the top electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

B2 cont.

53. ~~91~~. (Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

B

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, metal oxide dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit

wherein at least one electrode selected from the group consisting of the bottom electrode of the capacitor and the top electrode of the capacitor comprises tungsten nitride.

B2 cont.

54.
~~92.~~ (Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a

B

capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhomic crystalline structure;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

B2 cont

SS. ~~93.~~ (Amended) A memory module, comprising:

a support;

a plurality of leads extending from the support;

a command link coupled to at least one of the plurality of leads;

a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

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a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one, high temperature annealed metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

B2 cont.

56. ~~94.~~ (Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and

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an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

57. The system according to claim 56, wherein the electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer.

58. (Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

a row access circuit coupled to the array of memory cells;

B2 cont.

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a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

59.
~~97.~~ (Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having an orthorhomic crystalline structure;

B2 cont.

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

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60.
~~98.~~ (Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode, the buffer layer having a dielectric constant greater than the dielectric layer;

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

B2 Cont.

61.
~~99.~~ (Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory

B3

device comprises:

an array of memory cells, wherein at least one memory cell has a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one high temperature annealed, metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

B2 cont.

a row access circuit coupled to the array of memory cells;

a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

62. 100. (Amended) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

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a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

63. ~~101.~~ The system according to claim 62 ~~100~~, wherein the electrode selected from the group consisting of the first electrode and the second electrode includes a metal component that is the same as the metal component of the buffer layer.

B2 Cont. 64. ~~102.~~ (Amended) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

at least one tungsten oxide buffer layer, wherein each tungsten oxide buffer layer is interposed between the dielectric layer

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and an electrode selected from the group consisting of the first electrode and the second electrode.

65.
103. (Amended) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

B2 cont.

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein the metal oxide buffer layer has an orthorhomic crystalline structure.

66.
104. (Amended) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor

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die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode;

wherein the metal oxide buffer layer has a dielectric constant greater than the dielectric constant of the dielectric layer.

B2 Cont.

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~~105~~. (Amended) An electronic system, comprising:

a processor; and

a circuit module having a plurality of leads coupled to the processor, and further having a semiconductor die coupled to the plurality of leads, wherein the semiconductor die comprises:

an integrated circuit supported by a substrate and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices comprises a capacitor, the capacitor comprising:

a first electrode;

a second electrode;

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a single compound, dielectric layer interposed between the bottom electrode and the top electrode; and

at least one high temperature annealed, metal oxide buffer layer, wherein each metal oxide buffer layer is interposed between the dielectric layer and an electrode selected from the group consisting of the first electrode and the second electrode.

68.
106. (Amended) A capacitor, comprising:

an annealed bottom electrode;

a top electrode;

B2 cont.
a single compound, dielectric layer interposed between the top electrode and the bottom electrode; and

an annealed metal oxide buffer layer intermediate the dielectric layer and the bottom electrode.

69.
110. (Amended) A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes.

70.
111. The memory cell according to claim 110, wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

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71. 112. The memory cell according to claim 69 110, wherein the buffer layer has a orthorhomic crystalline structure.

72. 113. (Amended) A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a tungsten trioxide buffer layer interposed between the dielectric layer and one of the first and second electrodes.

B2 Cont.

73. 114. The memory cell according to claim 72 113, wherein the one electrode includes tungsten.

74. 115. The memory cell according to claim 73 114, wherein the buffer layer is grown by oxidizing the one electrode.

75. 116. (Amended) A memory cell comprising a capacitor and an access device, wherein the capacitor includes:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer interposed between the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

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76. 117. The memory cell according to claim 75 116, wherein the buffer layer is of the formula MO_x, and M is a metal component from a group consisting of tungsten, tantalum, zirconium, and hafnium.

77 118. (Amended) A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer intermediate the dielectric layer and one of the first and second electrodes.

B2 Cont.

78. 119. The memory cell according to claim 77 118, wherein the one electrode is a tungsten nitride and the buffer layer is a tungsten oxide.

79. 120. The memory cell according to claim 77 118, wherein the buffer layer has a orthorhomic crystalline structure.

80. 121. A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a dielectric layer interposed between the first electrode and the second electrode; and

a tungsten trioxide buffer layer interposed between the dielectric layer and one of the first and second electrodes.

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81. ~~122.~~ The memory cell according to claim 80 ~~121~~, wherein the one electrode includes tungsten.

82. ~~123.~~ The memory cell according to claim 81 ~~122~~, wherein the buffer layer is grown by oxidizing the one electrode.

83. ~~124.~~ (Amended) A processor and a memory cell electrically connected to said processor, wherein said memory cell includes a capacitor comprising:

a first electrode;

a second electrode;

a single compound, dielectric layer interposed between the first electrode and the second electrode; and

a metal oxide buffer layer interposed between the dielectric layer and one of the first and second electrodes, wherein the metal oxide buffer layer includes a refractory metal.

B2 Cont.

84. ~~125.~~ The memory cell according to claim 83 ~~124~~, wherein the buffer layer is of the formula MO_x, and M is a metal component from a group consisting of tungsten, tantalum, zirconium, and hafnium.

5. ~~126.~~ The capacitor of claim 1, wherein the dielectric layer directly adjoins the first electrode, and the metal oxide buffer layer directly adjoins the dielectric layer and the second electrode.

B3

6. ~~127.~~ The capacitor of claim 1, wherein the dielectric layer comprises a single layer.

B